What is claimed is:

1. An apparatus for constant amplitude coded bi-orthogonal demodulation, comprising:

a bi-orthogonal demodulation unit for demodulating received constant amplitude bi-orthogonal modulated data, canceling parity bits and then generating serial data;

an error detector for detecting the occurrence of an error while dividing the data demodulated in the bi-orthogonal demodulator into a plurality of groups of data and then outputting the serial data of the bi-orthogonal demodulator as demodulated data if an error does not occur;

an error bit polarity converter for sequentially converting bit polarities of data of groups with errors if the error detector detects the errors and converting the data of groups with errors and the data of groups with no errors into the serial data;

a constant amplitude coded bi-orthogonal modulator for performing the constant amplitude coded bi-orthogonal modulation for the output data of the error bit polarity converter;

a distance comparator for comparing bit-by-bit distances between the received bi-orthogonal modulated data and the constant amplitude coded bi-orthogonal modulated data of the constant amplitude coded bi-orthogonal modulator; and

a buffer for storing a number of serial data output from the error bit polarity converter and selectively outputting the corresponding serial data as demodulated data according to a control signal of the distance comparator.

2. The apparatus as claimed in claim 1, wherein the bi-orthogonal demodulation unit comprises:

a bi-orthogonal demodulator for demodulating the received bi-orthogonal modulated data;

a parity bit canceller for canceling the parity bits from the output data of the bi-orthogonal demodulator;

a plurality of switches for switching the data of the parity bit canceller according to the output signal of the error detector; and

a parallel to serial converter for receiving the switched data from the plurality of switches if the error detector has not detected errors and converting the data into serial demodulated data.

3. The apparatus as claimed in claim 1, wherein the error detector comprises:

first to third parity checkers for receiving the plurality of groups of data output from the bi-orthogonal demodulator, checking the parity bits, determining the occurrence of errors and controlling the plurality of switches; and

an OR gate for generating an error determining signal by performing an OR operation for output signals of the first to third parity checkers.

4. The apparatus as claimed in claim 1, wherein the error bit polarity converter comprises:

first to third bit polarity converters for receiving the data of the groups in which errors have occurred through the plurality of switches and converting their polarities;

a plurality of OR gates for performing OR operations for output data of the first to third bit polarity converters and data with no error switched in the plurality of switches; and

a parallel to serial converter for converting output data of the plurality of OR gates into serial data.

5. The apparatus as claimed in claim 1, wherein the constant amplitude coded bi-orthogonal modulator comprising:

a serial to parallel converter for converting the output data of the error bit polarity converter into a plurality of groups of data bits according to a data rate control signal;

a constant amplitude encoder for generating the parity bits for the respective groups by combining the plurality of groups of data bits converted in the serial to parallel converter;

an orthogonal code generator for generating a plurality of groups of orthogonal codes which are different from one another;

a plurality of bi-orthogonal modulation units for selecting one orthogonal code in each of the plurality of groups of orthogonal codes according to the plurality of groups of data bits and the parity bits of the respective groups, managing the polarities and performing the bi-orthogonal modulation; and

a parallel summer for parallel summing up output signals of the plurality of bi-orthogonal modulation units.

6. The apparatus as claimed in claim 5, wherein each of the plurality of bi-orthogonal modulation units comprises:

an orthogonal modulator for selecting as a polarity bit each one bit in each of the plurality of groups of data bits and a plurality of the parity bits for the respective groups and selecting one orthogonal code in each of the plurality of groups of orthogonal codes, corresponding to the remained bits except the selected one bit, and

a multiplier for multiplying the output signal of the orthogonal modulator by the selected polarity bit to adjust its polarity and outputting the multiplied and adjusted signal to the parallel summer.

7. The apparatus as claimed in claim 6, wherein the orthogonal modulator is a multiplexer.

8. The apparatus as claimed in claim 5, wherein the constant amplitude encoder generates the parity bits (r_0), (r_1), (r_2) by logically combining the data bits (b_0~b_2), (b_3~b_5), (b_6~b_8) of the respective groups according to the following formulas 2 to 4:

$$r_0 = \overline{b_0 \oplus b_3 \oplus b_6} \quad \ldots\ldots (2)$$

$$r_1 = b_1 \oplus b_4 \oplus b_7 \quad \ldots\ldots (3)$$

$$r_2 = b_2 \oplus b_5 \oplus b_8 \quad \ldots\ldots (4)$$

where $\oplus$ represents XOR.